Parallel Computer Structures

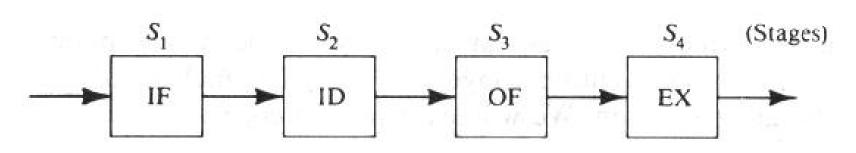


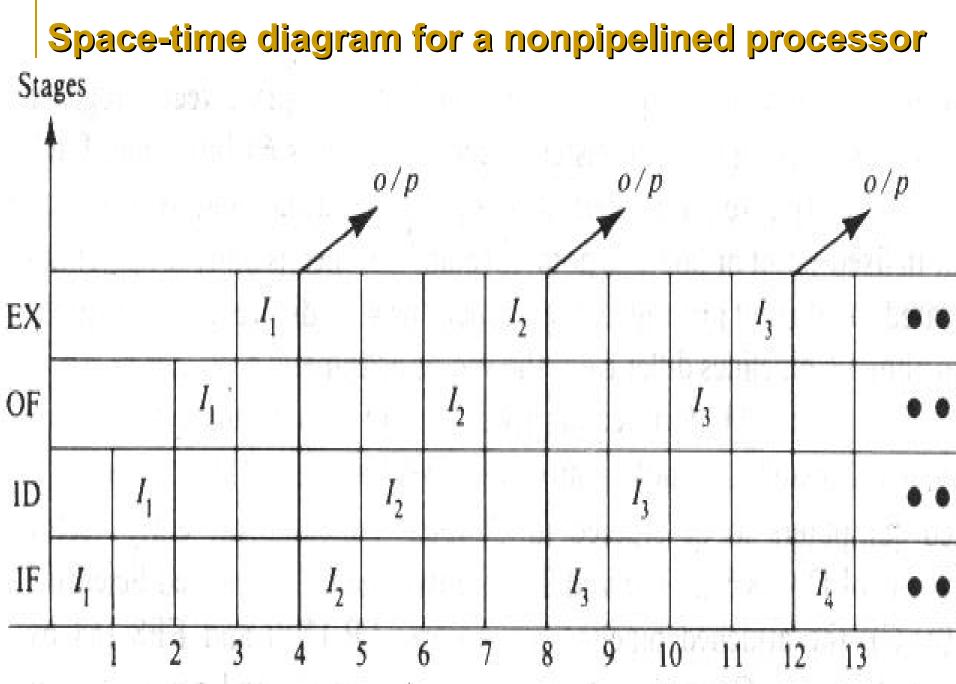
Parallel Computer Structures

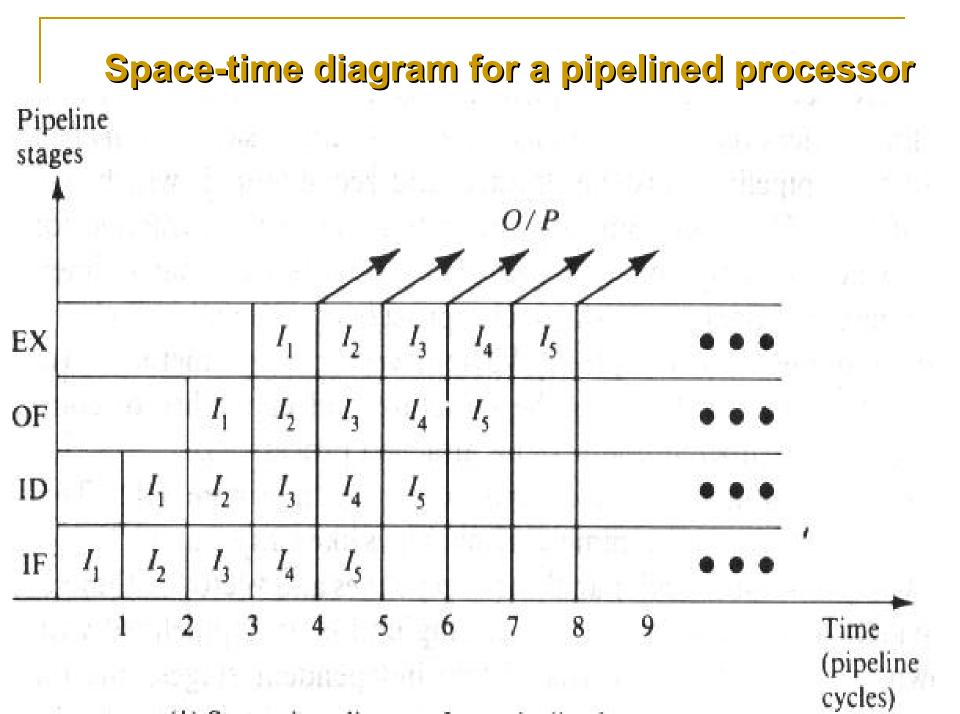
- Pipelined Computers :
 - overlapped computations
 - <u>temporal parallelism</u>.
- Array Processors :
 - multiple synchronized arithmetic logic units
 - □ <u>spatial parallelism</u>.
- Multiprocessor Systems :
 - <u>asynchronous parallelism</u>
 - set of interactive processors with shared resources.

Pipeline Computers

- Normally, four major steps to execute an instruction:
 - Instruction Fetch (IF)
 - Instruction Decoding (ID)
 - Operand Fetch (OF)
 - Execution (EX)

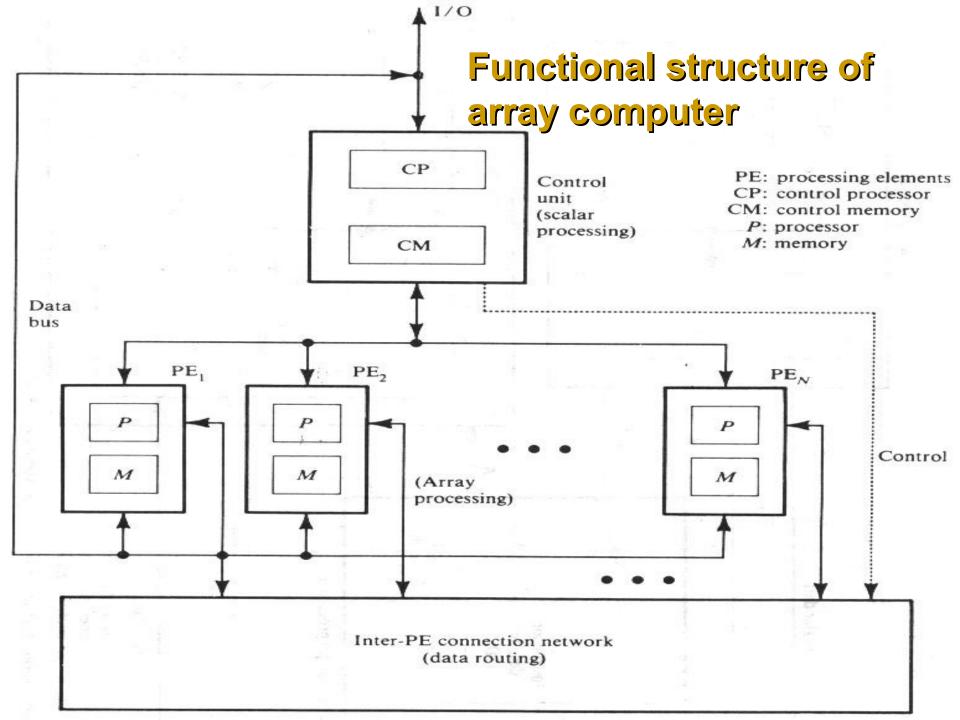






Array Computers

- A synchronous parallel computer
- Multiple arithmetic logic units
 - processing elements (PE)
 - operate in parallel.
- PEs are synchronized
 - perform the same function at the same time.
- Appropriate data routing mechanism must be established among the PEs.



Multiprocessor Systems

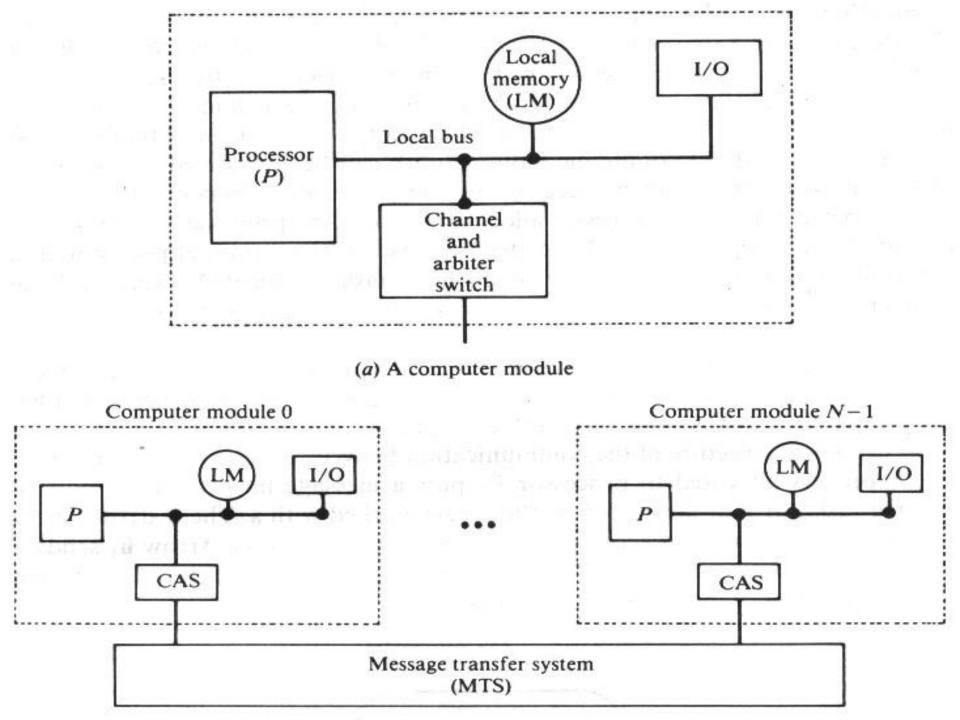
- A single computer that includes multiple processors (computer modules).
- All processors share memory modules, I/O channels and peripheral devices.
- Controlled by one operating system
 - provides interaction between processors and their programs.
- Local memory and private devices.



Processor communication

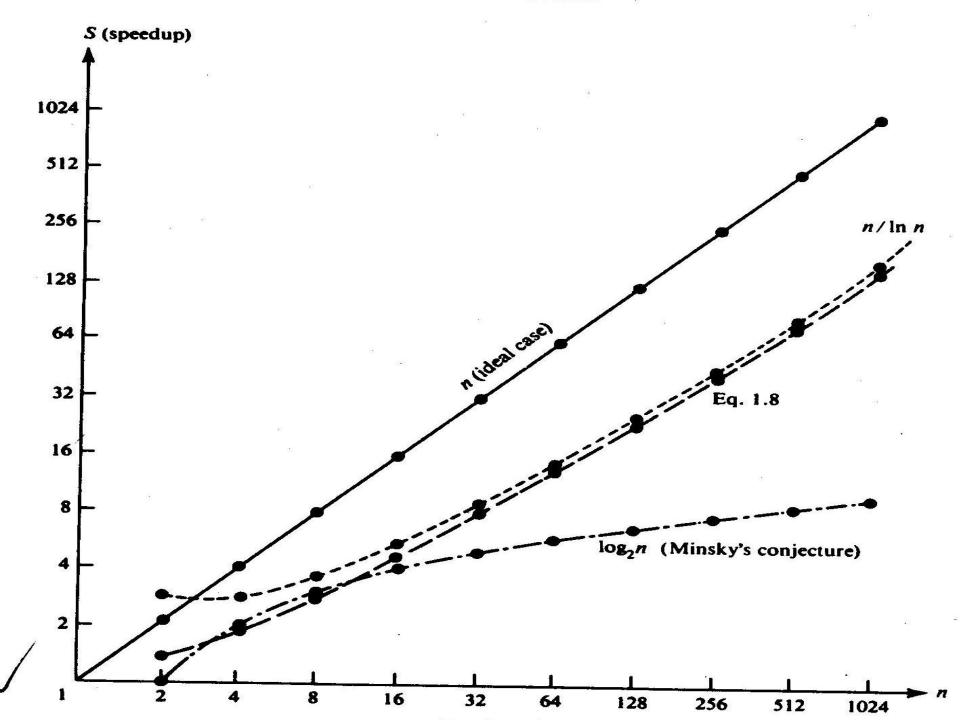
- sending messages
- sharing a common memory or through an interrupt network.
- Interconnections
 - Time-shared common bus
 - Crossbar switch network
 - Multiport memories





Performance of Parallel Computers

- Speedup of a parallel computer with n identical processors
 - n times faster than single processor.
- Speedup is much less(in practice)
 - some processors are idle.
- Actual speedup
 - Iower-bound log₂n (Minsky's conjecture)
 - upper bound *n/ln n*
- So Commercial processor system consists of only 2 or 4 processors.



T₁=1

- *f_i* probability of assigning the same problem to *i* processors.
- Average load = $d_i = 1/i$ per processor

$$f_i = 1/n.$$

Average time required to solve the problem on an n- processor system is $T_n = \sum_{i=1}^n f_i d_i = \frac{\sum_{i=1}^n \frac{1}{i}}{n}$

• Average speedup $S = \frac{T_1}{T_n} = \frac{n}{\sum_{i=1}^n \frac{1}{i}} \le \frac{n}{\ln n}$

Architectural Classification Schemes

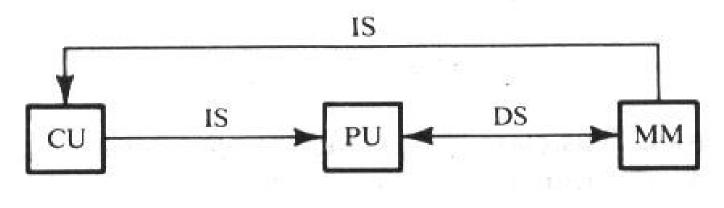


1. Flynn's Classification

- Multiplicity of data and instruction streams.
- Instruction stream
 - a sequence of instructions as executed by the machine.
- Data stream
 - a sequence of data including input, partial, or temporary results, called for by the instruction stream.
- Flynn's four machine organizations :
 SISD, SIMD, MISD, MIMD.



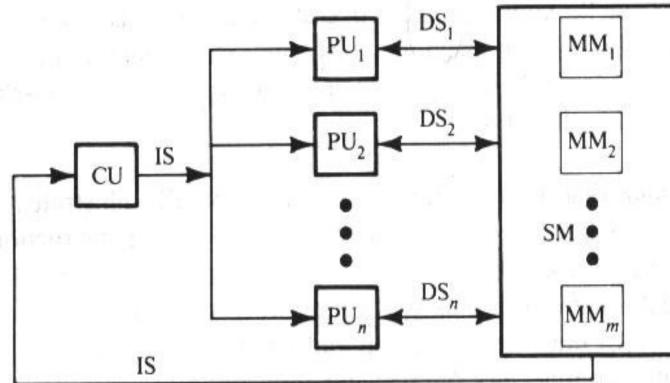
- Single Instruction stream-Single Data stream
- Instructions are executed sequentially but may be overlapped in their execution stages (pipelining).







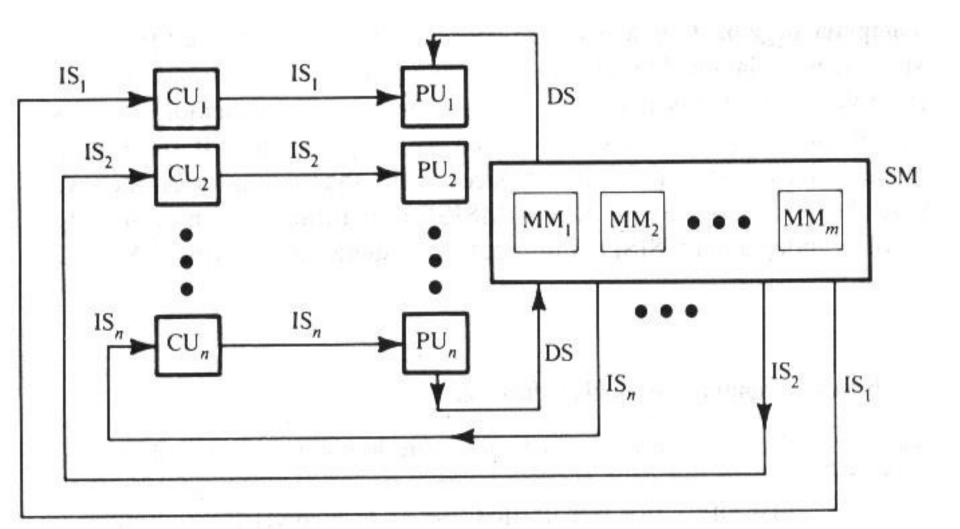
- Single Instruction stream-Multiple Data stream
- There are multiple PEs supervised by the same control unit.



CU: control unit PU: processor unit MM: memory module SM: shared memory IS: instruction stream DS: data stream

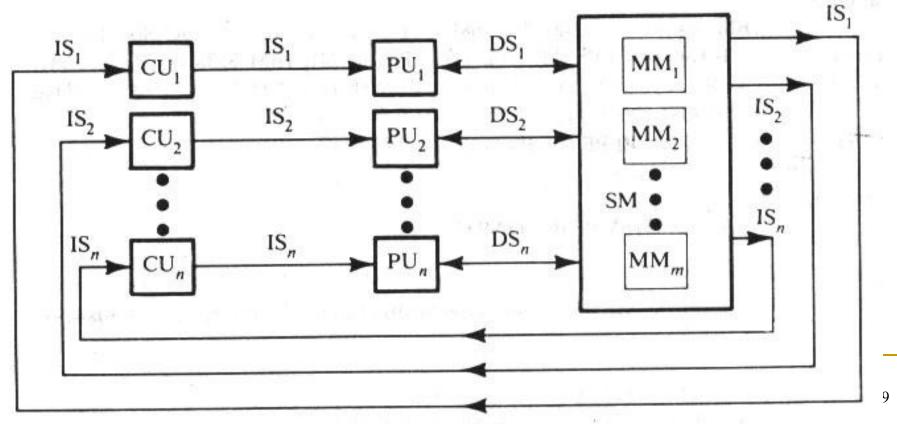


Multiple Instruction stream-Single Data stream





 Multiple Instruction stream-Multiple Data stream
 Multiprocessor systems and Multi- computer systems.



2. Feng's classification

- Use the degree of parallelism
- Maximum degree of parallelism
 - max: no: of bits that can be processed within a unit time (P).
- Average parallelism degree
- Utilization Rate

$$u = \frac{P_a}{P} = \frac{\sum_{i=1}^{T} P_i}{T.P}$$



- Max: parallelism degree, P(C) of a computer system C is P(C) = n.m
- Four type of processing methods
- 1. Word-serial and bit-serial (WSBS)
 - □ n=m=1
 - Bit serial processing as one bit is processed at a time.
- 2. <u>Word-parallel and bit-serial (WPBS)</u>
 - □ n=1, m>1
 - Bis(Bit-slice) processing as an m-bit-slice is processed at a time.

<u>Word-serial and bit-parallel (WSBP)</u> n>1, m=1

Word-slice processing as it processed one word of n-bits at a time.

4. Word-parallel and bit-parallel (WPBP)

- □ n>1, m>1
- Parallel processing as an array of (n x m) bits is processed at a time.



3. Handler's Classification

- Degree of parallelism and pipelining built in to the hardware structures of a computer system.
- Parallel pipeline processing is considered at three subsystem levels:
 PCU, ALU, BLC
- $T(X) = \langle K X K', D X D', W X W' \rangle$
- **Ex:**
- TI ASC <1, 4, 64 x 8>